In the claims:

1-17 (Cancelled)

18. (original) A base station that supports communications with a plurality of subscriber units in a CDMA wireless communication system, the base station comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a base station controller interface coupled to the processing circuitry; and

the base station supporting a power control channel comprising:

a plurality of power control bits, each power control bit corresponding to a reverse link common channel of the plurality of reverse link common channels and directing a respective subscriber unit to adjust its reverse link transmission power; and

a plurality of inhibit bits, each of the plurality of inhibit bits corresponding to a reverse link common channel of the plurality of reverse link common channels and indicating whether a dedicated burst mode has been scheduled for the reverse link common channel.

19. (previously presented) The base station of claim 18, wherein a power control bit of the plurality of power control bits are transmitted by the base station during a message capsule or preamble portion of a respective reverse link common channel.

20. (previously presented) The base station of claim 18, wherein an inhibit bit corresponding to a respective reverse link common channel is transmitted during an idle time of the respective reverse link common channel.

21. (original) A base station that supports communications with a plurality of subscriber units in a CDMA wireless communication system, the base station comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a base station controller interface coupled to the processing circuitry; and

the base station supporting a power control channel comprising:

a first power control/inhibit bit stream that corresponds to a first reverse link common channel; and

a second power control/inhibit bit stream that corresponds to a second reverse link common channel, the second power control/inhibit bit stream offset in relation to the first power control/inhibit bit stream.

22. (original) The base station of claim 21, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset.

23. (original) The base station of claim 21, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset.

24. (original) The base station of claim 21, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a varying offset that is based upon a counter value.

25. (original) The base station of claim 21, wherein the power control signal further comprises:

a third power control/inhibit bit stream that corresponds to a third reverse link common channel; and

a fourth power control/inhibit bit stream that corresponds to a fourth reverse link common channel.

26. (original) The base station of claim 25, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset;

the third power control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset; and

the fourth control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset.

27. (original) The base station of claim 25, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by a fixed offset.

28. (original) The base station of claim 25, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by another pseudo-random offset.

29. (original) The base station of claim 25, wherein:

a starting bit position is pseudo-randomly selected from a plurality of available bit positions; and

the first, second, third and fourth power control/inhibit bit streams are pseudo-randomly positioned based upon the starting bit position.

30. (previously presented) A base station that supports communications with a plurality of subscriber units in a CDMA wireless communication system, the base station comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a base station controller interface coupled to the processing circuitry; and

the base station supporting a common control channel comprising:

a common power control signal causing the subscriber units to manage their reverse link transmissions on a plurality of reverse link common channels, the common power control signal mapped to a first portion of a Walsh channel; and

a quick paging signal that sends pages to the plurality of subscriber units, the quick paging signal mapped to a second portion of the Walsh channel.

31. (original) The base station of claim 30, wherein:

the common power control signal is mapped to an in phase portion of the Walsh channel; and

the quick paging signal is mapped to a quadrature portion of the Walsh channel.

32. (original) The base station of claim 30, wherein:

the common power control signal is mapped to a quadrature portion of the Walsh channel; and

the quick paging signal is mapped to an in phase portion of the Walsh channel.

33. (previously presented) A subscriber unit that supports communications with a base station in a CDMA wireless communication system, the subscriber unit comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a user interface coupled to the processing circuitry; and

the subscriber unit decoding and processing a power control signal to extract a power control bit and an inhibit bit corresponding to a common channel used by the subscriber unit, the power control signal comprises:

a plurality of power control bits, each power control bit corresponding to a respective reverse link common channel of a plurality of reverse link common channels and directing a respective subscriber unit transmitting on the respective reverse link common channel to adjust its reverse link transmission power; and

a plurality of inhibit bits, each of the plurality of inhibit bits corresponding to a respective reverse link common channel of the plurality of reverse link common channels and indicating whether a dedicated burst mode has been scheduled for the respective reverse link common

channel.

34. (original) A subscriber unit that supports communications with a base station in a CDMA wireless communication system, the subscriber unit comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a user interface coupled to the processing circuitry; and

the subscriber unit decoding and processing a power control signal to extract a first power control/inhibit bit stream that corresponds to a first reverse link common channel, the power control signal comprising:

a first power control/inhibit bit stream that corresponds to a first reverse link common channel; and

a second power control/inhibit bit stream that corresponds to a second reverse link common channel, the second power control/inhibit bit stream offset in relation to the first power control/inhibit bit stream.

35. (original) The subscriber unit of claim 34, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset.

36. (original) The subscriber unit of claim 34, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset.

37. (original) The subscriber unit of claim 34, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a varying offset that is based upon a counter value.

38. (original) The subscriber unit of claim 34, wherein the power control signal further comprises:

a third power control/inhibit bit stream that corresponds to a third reverse link common channel; and

a fourth power control/inhibit bit stream that corresponds to a fourth reverse link common channel.

39. (original) The subscriber unit of claim 38, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset;

the third power control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset; and

the fourth control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset.

40. (original) The subscriber unit of claim 38, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by a fixed offset.

41. (original) The subscriber unit of claim 38, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by another pseudo-random offset.

42. (original) The subscriber unit of claim 38, wherein:

a starting bit position is pseudo-randomly selected from a plurality of available bit positions; and

the first, second, third and fourth power control/inhibit bit streams are pseudo-randomly positioned based upon the starting bit position.

43. (original) A subscriber unit that supports communications with a base station in a CDMA wireless communication system, the subscriber unit comprising:

an antenna;

a radio frequency interface coupled to the antenna;

a spreader/despreader coupled to the radio frequency interface;

a coder/decoder coupled to the spreader/despreader;

processing circuitry coupled to the coder/decoder;

memory coupled to the processing circuitry;

a user interface coupled to the processing circuitry; and

the subscriber unit decoding and processing a power control channel comprising:

a common power control signal mapped to a first portion of a Walsh channel; and

a quick paging signal that is mapped to a second portion of the Walsh channel.

44. (original) The subscriber unit of claim 43, wherein:

the common power control signal is mapped to an in phase portion of the Walsh channel; and

the quick paging signal is mapped to a quadrature portion of the Walsh channel.

45. (original) The subscriber unit of claim 43, wherein:

the common power control signal is mapped to a quadrature portion of the Walsh channel; and

the quick paging signal is mapped to an in phase portion of the Walsh channel.

46. (previously presented) A method for transmitting power control bits from a base station to a plurality of subscriber units in a code division multiple access wireless communication system, the common power control bits causing the subscriber units to manage their reverse link transmissions on a plurality of reverse link common channels, the method comprising:

determining a plurality of power control bits, each power control bit corresponding to a respective reverse link common channel of the plurality of reverse link common channels and directing a respective subscriber unit to adjust its reverse link transmission power;

determining a plurality of inhibit bits, each of the plurality of inhibit bits corresponding to a respective reverse link common channel of the plurality of reverse link common channels and indicating whether a dedicated burst mode has been scheduled for the reverse link common channel;

assembling the plurality of power control bits and the plurality of inhibit bits into a common bit stream; and

transmitting the common bit stream to the plurality of subscriber units.

47. (original) The method of claim 46, wherein power control bits corresponding to a reverse link common channel are transmitted during a message capsule portion of the reverse link common channel.

48. (original) The method of claim 46, wherein an inhibit bit corresponding to a reverse link common channel is transmitted during an idle time of the reverse link common channel.

49. (original) A method for transmitting power control bits from a base station to a plurality of subscriber units in a code division multiple access wireless communication system, the common power control bits causing the subscriber units to manage their reverse link transmissions on a plurality of reverse link common channels, the method comprising:

determining a first power control/inhibit bit stream that corresponds to a first reverse link common channel;

determining a second power control/inhibit bit stream that corresponds to a second reverse link common channel;

combining the first power control/inhibit bit stream with the second power control/inhibit bit stream into a common bit stream such that the second power control/inhibit bit stream is offset in relation to the first power control/inhibit bit stream; and

transmitting the combined bit stream on a forward link channel.

50. (original) The method of claim 49, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset.

51. (original) The method of claim 49, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset.

52. (original) The method of claim 49, wherein the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a varying offset that is based upon a counter value.

53. (original) The method of claim 49, further comprising:

determining a third power control/inhibit bit stream that corresponds to a third reverse link common channel; and

determining a fourth power control/inhibit bit stream that corresponds to a fourth reverse link common channel.

54. (original) The method of claim 53, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a fixed offset;

the third power control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset; and

the fourth control/inhibit bit stream is offset from the first power control/inhibit bit by a fixed offset.

55. (original) The method of claim 53, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by a fixed offset.

56. (original) The method of claim 53, wherein:

the second power control/inhibit bit stream is offset from the first power control/inhibit bit stream by a pseudo-random offset; and

the fourth power control/inhibit bit stream is offset from the third power control/inhibit bit by another pseudo-random offset.

57. (original) The method of claim 53, wherein:

a starting bit position is pseudo-randomly selected from a plurality of available bit positions; and

the first, second, third and fourth power control/inhibit bit streams are pseudo-randomly positioned based upon the starting bit position.

58-60. (cancelled)